REMARKS

The Examiner requested that Applicants provide an English translation of the Nikkei Electronics reference cited in the PTO-1149 previously submitted on November 20, 1998. Applicants submit herewith a partial English language translation of the relevant sections of this publication. Accordingly, the Examiner is requested to appropriately initial and forward a copy to Applicants, a copy of the PTO-1449 form indicating consideration of this cited prior art. It is respectfully requested that the document be expressly considered during the prosecution of this application, and that the document be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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PARTIAL ENGLISH LANGUAGE TRANSLATION OF NIKKEI ELECTORNICS 1994.2.14

...omitted...

(P.68) It is readily understand that the mounting of BGA is easy. However, the junction of soldered portion is not visible. Is there really no problem even without visible monitoring.

...omitted...

For QFP and other packages with lead terminals, visual monitoring of the appearance can find a failure such as simple mounting of lead on solder without forming junction.

...omitted...

(P. 69) For BGA, it is considered that the solder junction can be reliably formed and mere electrical test would be sufficient.

...omitted...

(PP.70-71) SCAN PATH AND OTHER CONTRIVANCE ARE EXPECTED

Even an in-circuit test methodology is associated with a problem. Plastic BGA has terminals placed on the bottom, and probe pins of the in-circuit tester can not contact the terminals. Some contrivance is required such as provision of a test-dedicated pad on a mounting board and utilization of a scan design methodology *.

(P.70) *SCAN DESIGN METODOLOGY

One of designing methodology for enhancing the testability of IC sequential circuit. A test-dedicated circuit is added to a storage element such as a flip flop, to make easy an access through an external terminal. The testing of a sequential circuit can be made equivalent to the testing of a combinational circuit, and the generation of test pattern can be made simplified.

(P.71) **JTAG (Joint Test Action Group)

An association that proposed a standard specification of a mounting board testing approach of the boundary scan test. Apparatus makers and semiconductor makers of Europe and United States of America join the Group. The boundary scan is an expanded version of the scan test methodology to the test of the mounting circuit board.